CLAIMS

What is claimed:

Sub A1

1. A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material;

depositing a metal layer over the substrate and the alignment component;

reacting the metal layer with the semiconductor material of the substrate to form two silicide regions substantially extending up to the alignment component on opposing sides of the alignment component; and

replacing the alignment component with a conductive gate substantially extending up to the silicide regions.

2. The method of claim 1 wherein the alignment component is non-conductive.

3. The method of claim 2 wherein the alignment component is made of a material selected from the group consisting of a silicon oxide and silicon nitride.

4. The method of claim 1 wherein the alignment component is made of a material which does not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

5. The method of claim 1 wherein the alignment component has a thickness of between 1000Å and 2500Å.

6. The method of claim 1 wherein the alignment component is less than 0.10 microns wide.

7. The method of claim 1 wherein the metal layer is selected from the group consisting of a material comprising tungsten, cobalt and titanium..

8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å thick.

9. The method of claim 1 wherein the silicide regions have lower surfaces located lower than a lower surface of the alignment component, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate.

10. The method of claim 1 wherein the alignment component is replaced with the gate according to a method comprising:

depositing a layer over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed;

etching the alignment component to leave an opening in the first layer; and

disposing a gate within the opening.

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11. The method of claim 10 wherein, after etching of the alignment component, the silicide regions extend substantially up to the opening.

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12. The method of claim 10 wherein the alignment component and the layer are made of different materials, one being made of a silicon oxide and the other being made of silicon nitride.

13. The method of claim 1 wherein the gate is formed according to a method comprising:

depositing a gate dielectric layer; and

forming a gate electrode on the gate dielectric layer.

14. The method of claim 13 wherein the gate dielectric layer is less than 10Å thick.

15. The method of claim 13 wherein the gate electrode is made out of a metal.

16. The method of claim 1, further comprising:

forming doped regions which extend from the silicide regions in underneath the gate.

17. The method of claim 13 wherein the gate dielectric layer has a dielectric constant of at least 100.

18. The method of claim 13 wherein the gate dielectric layer comprises a material selected from the group consisting of strontium titanate, and barium strontium titanate.

19. The method of claim 17 wherein the gate electrode comprises a material selected from the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.

20. A transistor comprising:

a substrate of a semiconductor material;

a gate on the substrate, the gate having a gate dielectric layer, on the substrate, which is less than 100 Å thick, and a gate electrode on the gate dielectric layer; and

two silicide regions on opposing sides of the gate and substantially extending up to the gate.

21. The transistor of claim 20 wherein the silicide regions have lower surfaces located lower than a lower surface of the gate, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate wherein the substrate has the same type dopant from the one silicide region to the other silicide region.

22. The transistor of claim 20 wherein the gate has a gate length of less than 0.10 microns.

23. The transistor of claim 20 wherein the gate comprises:

a spacer wall between the gate electrode and one of the silicide regions, the spacer wall being less than 100 Å thick.

24. The transistor of claim 20 wherein a single layer forms both the gate dielectric layer and the spacer wall.

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25. The transistor of claim 20, further comprising:

a respective doped region which extends from a respective silicide region in underneath the gate.